

What is claimed is:

1. A semiconductor integrated circuit comprising:

a first thin film transistor formed on a substrate, said first thin film transistor having a first gate insulating film and a first gate electrode; and

5 a second thin film transistor formed on said substrate, said second thin film transistor having a second gate insulating film and a second gate electrode,

wherein a variation of a first voltage applied to said first gate electrode is smaller than a variation of a second voltage applied to a second gate electrode, and

10 wherein a thickness of said first gate insulating film is 80 % or less of a thickness of said second gate insulating film.

2. A semiconductor integrated circuit comprising:

a first thin film transistor formed on a substrate, said first thin film transistor having a first gate insulating film and a first gate electrode; and

15 a second thin film transistor formed on said substrate, said second thin film transistor having a second gate insulating film and a second gate electrode,

wherein a variation of a first voltage applied to said first gate electrode is smaller than a variation of a second voltage applied to a second gate electrode, and

20 wherein at least one layer of another insulating layer is used for said second gate insulating film in addition to an insulating layer composing said first gate insulating film.

3. A semiconductor integrated circuit comprising:

a first thin film transistor formed on a substrate, said first thin film transistor having a first gate insulating film and a first gate electrode; and

25 a second thin film transistor formed on said substrate, said second thin film transistor having a second gate insulating film and a second gate electrode, wherein said second gate insulating film includes a first insulating layer and a second insulating layer,

wherein a variation of a first voltage applied to said first gate electrode is smaller than a variation of a second voltage applied to a second gate electrode,

wherein said first insulating layer is said first gate insulating film and said second insulating layer is formed by a different process from said first insulating layer.

5        4. A semiconductor integrated circuit comprising:

        a first thin film transistor formed on a substrate, said first thin film transistor having a first gate insulating film and a first channel region; and

        a second thin film transistor formed on said substrate, said second thin film transistor having a second gate insulating film and a second channel region,

10        wherein a first thickness of said first gate insulating film is 80 % or less of a second thickness of said second gate insulating film, and

        wherein a first length of said first channel region is 80% or less of a second length of said second channel region.

5. A circuit according to claims 1 wherein said first thin film transistor composes  
15 a logic circuit and said second thin film transistor composes a matrix circuit.

6. A circuit according to claims 1 wherein said first thin film transistor composes a logic circuit and said second thin film transistor composes a high withstand voltage switching circuit.

7. A circuit according to claims 1 wherein said first thin film transistor composes  
20 a logic circuit and said second thin film transistor composes a buffer circuit.

8. A circuit according to claims 1 wherein said second thin film transistor comprises at least a low concentration impurity region formed by utilizing a difference of the thickness of the gate insulating films.

9. A circuit according to claim 3 wherein said first insulating layer has a

different chemical component from said second insulating layer.

10. A circuit according to claim 3 wherein either one of said first insulating layer or said second insulating layer is formed by thermal oxidation.

11. A method for fabricating a semiconductor integrated circuit, said method  
5 comprising the steps of:

forming a first thin film semiconductor region for a first thin film transistor and a second thin film semiconductor region for a second thin film transistor;

forming a first insulating layer covering both of said first and second thin film semiconductor regions;

10 selectively removing said first insulating layer to remove all of said first insulating layer covering at least said second thin film semiconductor region; and

forming a second insulating layer covering both of said first and second thin film semiconductor regions.

12. A method for fabricating a semiconductor integrated circuit, said method  
15 comprising the steps of:

forming a first thin film semiconductor region for a first thin film transistor and a second thin film semiconductor region for a second thin film transistor;

forming a first insulating layer covering both of said first and second thin film semiconductor regions;

20 forming a second insulating layer covering said first insulating layer; and  
selectively removing said second insulating layer to remove all of said second insulating layer covering at least said second thin film semiconductor region.

13. A method for fabricating a semiconductor integrated circuit, said method comprising the steps of:

25 forming a first thin film semiconductor region for a first thin film transistor and a second thin film semiconductor region for a second thin film transistor;

selectively forming a first insulating layer covering both of said first and second thin film semiconductor regions except a portion of at least said second thin film semiconductor region; and

forming a second insulating layer covering both of said first and second  
5 thin film semiconductor regions.

14. A method according to claims 11 wherein said first insulating layer is formed by thermal oxidation.

15. A method according to claims 11 wherein said second thin film transistor composes a logic circuit and said first thin film transistor composes a matrix circuit.

10 16. A method according to claims 11 wherein said second thin film transistor composes a logic circuit and said first thin film transistor composes a high withstand voltage switching circuit.

17. A method according to claims 11 wherein said second thin film transistor composes a logic circuit and said first thin film transistor composes a buffer circuit.

15 18. A method according to claims 11 further comprising the steps of:  
forming a first gate electrode and a second gate electrode, said first gate electrode having a different width from said second gate electrode,  
forming a source region, a drain region and channels by doping, said channels having different lengths.

20 19. A circuit according to claims 2 wherein said first thin film transistor composes a logic circuit and said second thin film transistor composes a matrix circuit.

20. A circuit according to claims 3 wherein said first thin film transistor composes a logic circuit and said second thin film transistor composes a matrix circuit.

21. A circuit according to claims 4 wherein said first thin film transistor composes a logic circuit and said second thin film transistor composes a matrix circuit.

22. A circuit according to claims 2 wherein said first thin film transistor composes a logic circuit and said second thin film transistor composes a high  
5 withstand voltage switching circuit.

23. A circuit according to claims 3 wherein said first thin film transistor composes a logic circuit and said second thin film transistor composes a high withstand voltage switching circuit.

24. A circuit according to claims 4 wherein said first thin film transistor  
10 composes a logic circuit and said second thin film transistor composes a high withstand voltage switching circuit.

25. A circuit according to claims 2 wherein said first thin film transistor composes a logic circuit and said second thin film transistor composes a buffer circuit.

26. A circuit according to claims 3 wherein said first thin film transistor  
15 composes a logic circuit and said second thin film transistor composes a buffer circuit.

27. A circuit according to claims 4 wherein said first thin film transistor composes a logic circuit and said second thin film transistor composes a buffer circuit.

28. A circuit according to claims 2 wherein said second thin film transistor comprises at least a low concentration impurity region formed by utilizing a  
20 difference of the thickness of the gate insulating films.

29. A circuit according to claims 3 wherein said second thin film transistor

comprises at least a low concentration impurity region formed by utilizing a difference of the thickness of the gate insulating films.

30. A circuit according to claims 4 wherein said second thin film transistor comprises at least a low concentration impurity region formed by utilizing a  
5 difference of the thickness of the gate insulating films.

31. A method according to claims 12 wherein said second thin film transistor composes a logic circuit and said first thin film transistor composes a matrix circuit.

32. A method according to claims 13 wherein said second thin film transistor composes a logic circuit and said first thin film transistor composes a matrix circuit.

10 33. A method according to claims 12 wherein said second thin film transistor composes a logic circuit and said first thin film transistor composes a high withstand voltage switching circuit.

34. A method according to claims 13 wherein said second thin film transistor composes a logic circuit and said first thin film transistor composes a high withstand  
15 voltage switching circuit.

35. A method according to claims 12 wherein said second thin film transistor composes a logic circuit and said first thin film transistor composes a buffer circuit.

36. A method according to claims 13 wherein said second thin film transistor composes a logic circuit and said first thin film transistor composes a buffer circuit.

20 37. A method according to claims 12 further comprising the steps of:  
forming a first gate electrode and a second gate electrode, said first gate electrode having a different width from said second gate electrode,

forming a source region, a drain region and channels by doping, said channels having different lengths.

38. A method according to claims 13 further comprising the steps of:

forming a first gate electrode and a second gate electrode, said first gate  
5 electrode having a different width from said second gate electrode,

forming a source region, a drain region and channels by doping, said channels having different lengths.

39. A device according to claim 1 wherein said first thin film transistor composes  
a first circuit for high operating speed and said second thin film transistor composes a  
10 second circuit for high withstand voltage.